REMARKS

This is a full and timely response to the outstanding Office Action mailed April 5, 2005. Claims 1 and 5 - 12 remain pending, claims 2 – 4 and 13 – 32 having been withdrawn. In particular, Applicant has amended claim 1. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Rejections Under 35 U.S.C. 112

The Office Action indicates that claims 11 and 12 are rejected under 35 U.S.C. 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. In this regard, Applicant has amended claim 11 and respectfully asserts that the rejection has been accommodated.

Rejections Under 35 U.S.C. 102(e)

The Office Action indicates that claims 1, 5 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by *Solomon*. Applicant respectfully traverses the rejection.

In this regard, the Office Action indicates that:

> Solomon et al. discloses a method for forming a gate stack having improved electrical properties in a gate structure forming process comprising the steps of: providing a semiconductor substrate (12); forming a metal oxide layer (16) (col.3, lines 55-60) over an exposed portion of the semiconductor substrate; and, forming a layer of electrode (18) over the metal oxide layer in a nitrogen containing ambient (col. 5 lines 15-20).

(Office Action).

However, *Solomon* actually discloses that "FGA treatments were then performed on additional specimens formed to have an aluminum-tungsten electrode stack by annealing in an inert ambient, such as nitrogen." (*Solomon* at col. 5 lines 15-20) and "Finally, the gate electrode

18 is formed by a metal layer." (*Solomon* at col. 3 lines 61-62). Thus, the present claims clearly distinguish over *Solomon*.

In this regard, Applicant has amended claim 1 to recite:

> 1. A method for forming a gate stack having improved electrical properties in a gate structure forming process comprising the steps of:
> providing a semiconductor substrate;
> forming a metal oxide layer over an exposed portion of the semiconductor substrate; and
> ***forming a silicon-containing electrode layer over the metal oxide layer in a nitrogen containing ambient.***

(Emphasis Added).

Applicant respectfully asserts that *Solomon* is legally deficient for the purpose of anticipating claim 1. Specifically, Applicant respectfully assert that *Solomon* does not teach or otherwise disclose at least the features/limitation emphasized above in claim 1. Therefore, Applicants respectfully assert that the rejection is improper and requests that the rejection of claims 1, 5 and 8 under 35 U.S.C. 102 be removed.

Rejections Under 35 U.S.C. 103(a)

The Office Action indicates that claims 1 and 5 - 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Hegde* in view of *Thakur*. The Office Action also indicates that claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Hegde* in view of *Yu*. Applicant respectfully traverses the rejections.

In this regard, the Office Action indicates that:

> Hegde et al. discloses a method for forming a gate stack having improved electrical properties in a gate structure forming process comprising the steps of: providing a semiconductor substrate (12); forming a metal oxide layer (26) (a HfO_2 layer with a dielectric constant of greater than about 20. Col.2 lines 40-51) over an exposed portion of the semiconductor substrate; and, forming a layer of electrode (a polysilicon layer 16)(col.2 lines 5-6) over the metal oxide layer. See Fig. 1 and Fig. 2. Thakur et al. teaches that a polysilicon gate electrode (20) is doped with impurities in a nitrogen containing ambient in

> order to reduce the sheet resistance of the gate electrode. (abstract and col. 4 lines 22-31) It would have been obvious to one of ordinary skill in the art to form the gate electrode in a nitrogen containing ambient as taught by Thakur et al. in Hegde et al.'s device in order to reduce the sheet resistance of the gate electrode.

(Office Action).

However, *Thakur* discloses that "In forming polysilicon layer 20, the first gas preferably comprises silane, disilane, or dichlorosilane, though other gases known to one of ordinary skill in the art may also be employed." (*Thakur* at col. 3 line 67 to col. 4 line 2). Additionally, *Thakur* discloses

> In doping polysilicon layer 20 with material 22, the second gas comprises ambient characteristics. Ambient characteristics refer to the creation of an atmosphere or ambient which is essentially free of oxygen. This usually requires the flowing of a gas into the chamber. Gases used to create ambient characteristics include, but are not limited to: argon (Ar), nitrogen (N_2), and ammonia (NH_3).

(*Thakur* at col. 4 lines 22-29).

As described in detail below, the present claims clearly distinguish over these teachings.

In this regard, Applicant has amended claim 1 to recite:

> 1. A method for forming a gate stack having improved electrical properties in a gate structure forming process comprising the steps of:
> providing a semiconductor substrate;
> forming a metal oxide layer over an exposed portion of the semiconductor substrate; and
> ***forming a silicon-containing electrode layer over the metal oxide layer in a nitrogen containing ambient.***

(Emphasis Added).

Applicant respectfully assert that *Hegde* and *Thakur*, either individually or in combination, are legally deficient for the purpose of rendering claim 1 unpatentable. Specifically, Applicant respectfully asserts that neither, nor a combination, of the cited references teaches or reasonably suggests at least the features/limitations emphasized above in claim 1. Therefore, Applicant respectfully asserts that claim 1 is in condition for allowance.

Since claims 5 – 9 and 11 - 12 are dependent claims that incorporate the limitations of claim 1, Applicant respectfully asserts that these claims also are in condition for allowance. Additionally, these claims recite other limitations that can serve as an independent basis for patentability.

Moreover, claim 10 is a dependent claim that incorporates the limitations of claim 1. In that the combination of *Hegde* and *Yu* does not teach or reasonably suggest at least the features/limitations emphasized above in claim 1, Applicant respectfully asserts that claim 11 also is in condition for allowance.

Cited Art Made of Record

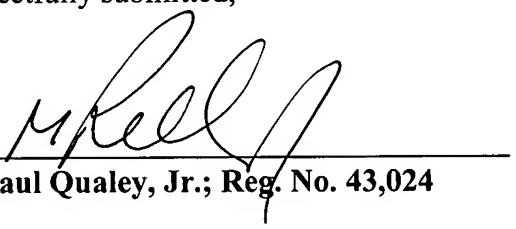
The cited art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

For at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,



M. Paul Qualey, Jr.; Reg. No. 43,024

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.
Suite 1750
100 Galleria Parkway N.W.
Atlanta, Georgia 30339
(770) 933-9500